WE CLAIM:

1. A processor comprising:

Intel Architecture-32 (IA-32) instruction set decoding logic; and

an expanded logical register set, coupled to said IA-32 instruction set, said expanded logical register set including more than eight logical registers of a first type.

2. The processor of claim 1, wherein said expanded logical register set includes up to sixteen logical registers of a first type.

3. The processor of claim 1, wherein said expanded logical register set includes up to thirty-two logical registers of a first type.

4. The processor of claim 1, wherein the more than eight logical registers of a first type include more than eight logical general integer registers.

5. The processor of claim 1, wherein the more than eight logical registers of a first type include more than eight logical MMX® technology registers.

6. The processor of claim 1, wherein the more than eight logical registers of a first type include more than eight logical SIMD (single instruction multiple data) floating-point registers.

7. The processor of claim 1, further comprising:

expanded register set decoding logic, coupled to said IA-32 instruction set decoding logic, to determine that an instruction includes an at least four-bit register identifier, the four-bit register identifier to specify one logical register of said expanded logical register set.

8. The processor of claim 7, wherein said expanded register set decoding logic is to decode an at least four-bit register identifier.

9. The processor of claim 8, wherein said expanded register set decoding logic is to decode the at least four-bit register identifier based at least in part on at least four bits of a scale index base (SIB) byte of the instruction.

10. The processor of claim 9, wherein said expanded register set decoding logic is to decode the at least four bit register identifier based at least in part on at least one bit of a scale field of the scale index base (SIB) byte of the instruction.

11. The processor of claim 7, wherein said expanded register set decoding logic is to decode an at least five bit register identifier.

12. The processor of claim 11, said expanded register set decoding logic is to decode the at least five bit register identifier based at least in part on five bits of a scale index base (SIB) byte of the instruction.

13. The processor of claim 12, wherein said expanded register set decoding logic is to decode the at least five-bit register identifier based at least in part on two bits of a scale field of the scale index base (SIB) byte of the instruction.

14. A processor comprising:

decoder logic to decode Intel Architecture-32 (IA-32) instructions; and

means for decoding an instruction that specifies a logical register of an expanded logical register set, the expanded logical register set including more than eight logical registers.

15. The processor of claim 14, wherein said means for decoding includes means for decoding an at least four-bit register identifier within the instruction.

16. The processor of claim 14, wherein said means for decoding includes means for decoding the at least four-bit register identifier within the instruction based on at least one bit within a scale field of a scale index base (SIB) byte of the instruction.

17. A method to access an expanded logical register set of a processor, the method comprising:

determining that a mod field of a ModR/M byte of an Intel Architecture-32 (IA-32) instruction contains a value selected from the values of 01B, 10B, and 00B;

determining that an r/m field of the ModR/M byte of the IA-32 instruction contains a value of 100B;

determining that an index field of a scale index base (SIB) byte contains a value of 100B; and

decoding an at least four-bit logical register identifier.

18. The method of claim 17, wherein decoding an at least four-bit logical register identifier is based at least in part on at least one bit of a scale field of a scale index base (SIB) byte of the IA-32 instruction.

19. The method of claim 17, wherein decoding an at least four-bit logical register identifier includes decoding an at least five-bit logical register identifier.

20. The method of claim 19, wherein decoding an at least five-bit logical register identifier is based at least in part on two bits of a scale field of a scale index base (SIB) byte of the IA-32 instruction.

21. A processor comprising:

a logical register set including more than eight logical registers of a first type;

instruction decoding logic coupled to the logical register set, said instruction decoding logic including:

a first comparator to determine that a mod field comparator to a ModR/M byte of an Intel Architecture-32 (IA-32) instruction contains a value selected from the values of 01B, 10B, and 00B;

a second comparator to determine that an r/m field of the ModR/M byte of the IA-32 instruction contains a value of 100B;

a third comparator to determine that an index field of a scale index base (SIB) byte contains a value of 100B; and

a decoder to decode an at least four-bit logical register identifier.

22. The processor of claim 21, wherein the decoder to decode an at least four-bit logical register identifier is to decode the at least four-bit logical register identifier based at least in part on at least one bit of a scale field of a scale index base (SIB) byte of the IA-32 instruction.